SIEMENS

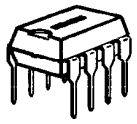
Nonvolatile Memory 1-Kbit E²PROM

SDE 2506

Preliminary DataMOS IC

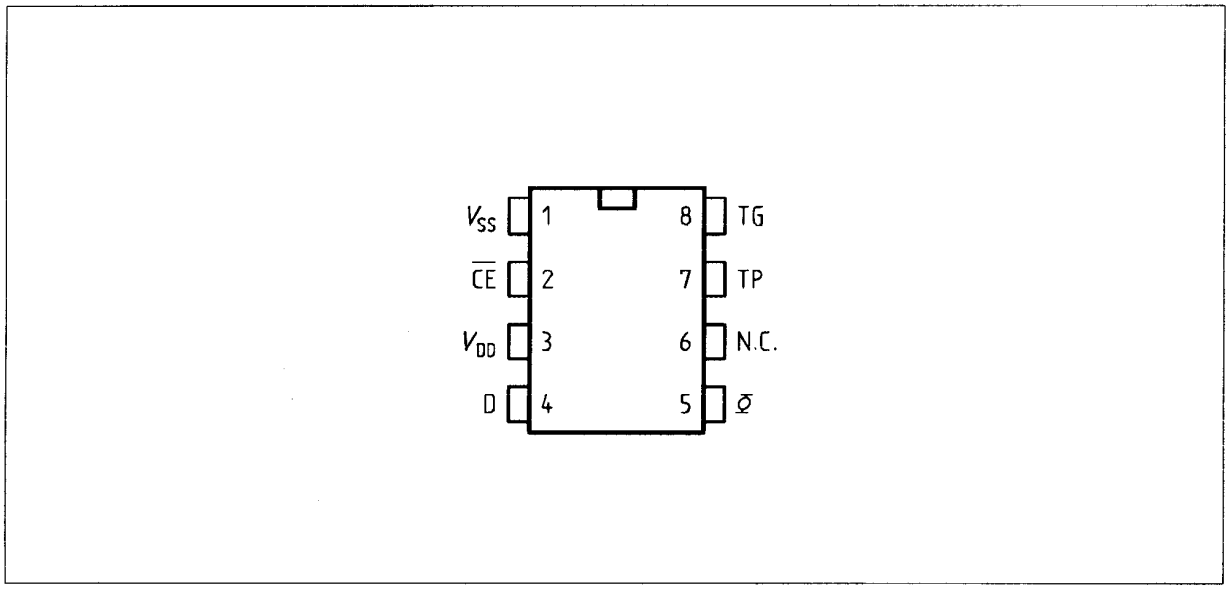
Features

- Word-organized reprogrammable nonvolatile memory in n-channel floating-gate technology
- 128 x 8-bit organization
- 5 V supply voltage
- 3 lines processor interface for data transfer and chip control
- Data input (8 bits), address input (7 bits), control information input (1 bit) and data output are serial
- More than 10^5 reprogramming cycles per address
- Data retention longer than 10 years (operating temperature range)
- Unlimited number of read-out operations without refresh
- 5 ms erase/write cycle
- Extended temperature range from – 40 to 110 °C



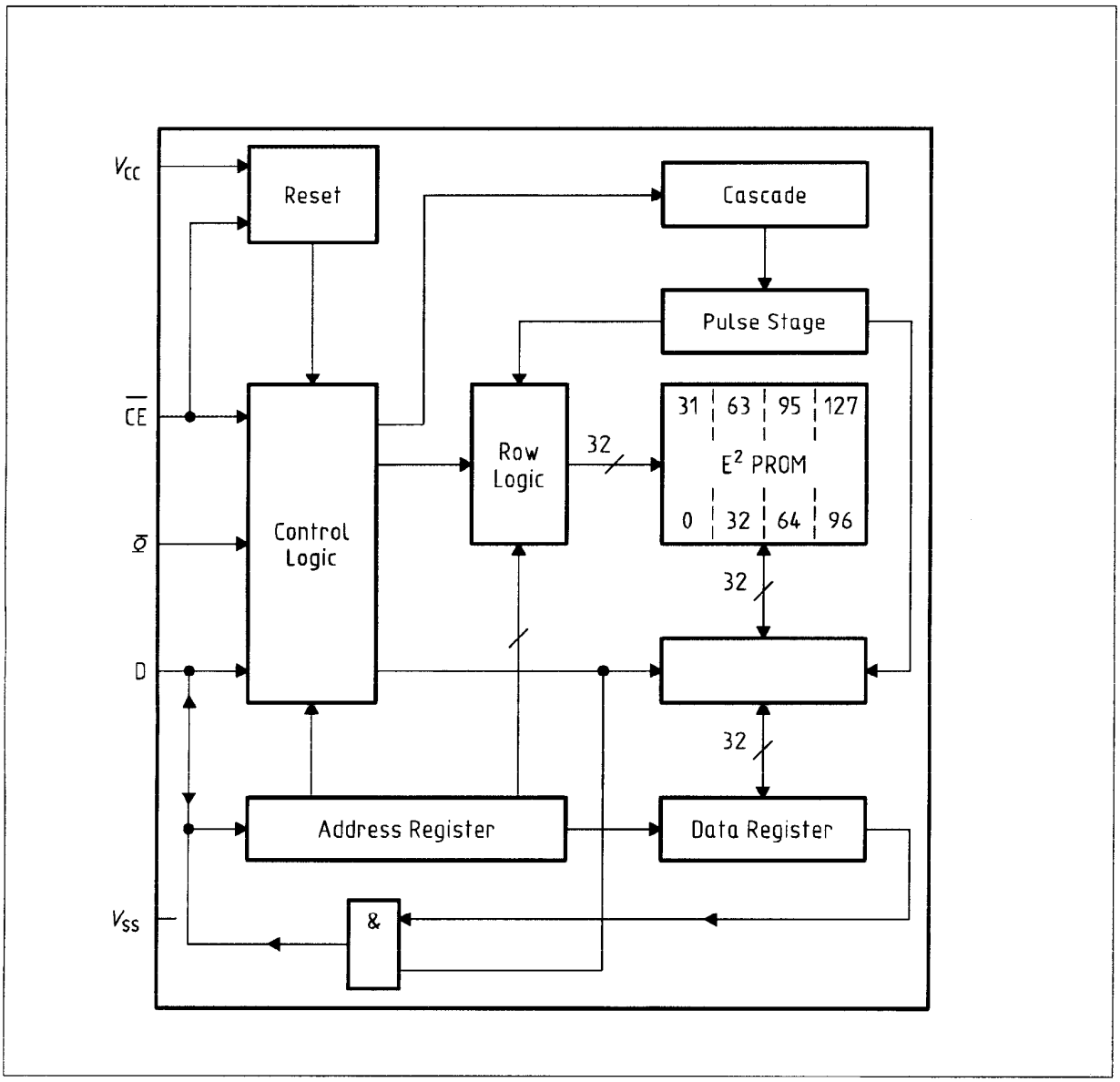
P-DIP-8-1

Pin Configurations
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	$\overline{CE}$ = 1 for data input/output, $\overline{CE}$ = 0 for reprogramming
3	V_{DD}	+ 5 V supply voltage
4	D	Data input/output bidirectional data line For reprogramming D = 1 erase, D = 0 write
5	Φ	Clock
6	N.C.	Not connected
7	TP	Test input, at V_{SS}
8	TG	Test input, remains open



Block Diagram

Circuit Description

Data Transfer and Chip Control

Three lines having several functions each are required for data transfer between control processor and E^2PROM memory.

a) Data line D
- bidirectional serial data transfer
- serial address input
- clocked input of a control information
- direct control input

b) Clock line Φ
- data input, address input and control bit input
- data output
- start read-out with takeover of data from memory in shift register or start data-change during reprogramming

c) Chip enable line $\overline{EC}$
- chip reset and data input (active high)
- chip enable (active low)

Prior to activating the chip, the data, address and control information is clocked in via the bidirectional data bus. These data are maintained in the shift register during reprogramming and read-out up to the second clock pulse. The following data formats have to be input:

a) Memory read-out: one 8-bit control word, consisting of
- 7 address bits A0 to A6 (at first A0 being LSB)
- 1 control bit, SB = "0", after A6

b) Memory reprogramming (erasure and/or writing) 16-bit input information, consisting of
- 8 bits D0 to D7 new memory information (at first D0 being LSB)
- 7 bits A0 to A6 address information (at first A0 being LSB after D7)
- 1 bit control information, SB = "1", after A6

Memory Read-Out

After data input and with SB = "0" the read-out operation of the selected word address is started by the transition of $\overline{CE}$ from "1" to "0". The information being on the data line during chip enable is of no influence.

With the first clock pulse after $\overline{CE}$ = "0" the data word is taken over from the selected memory address into the shift register. After termination of the first Φ pulse the data output is in the low impedance state. With every following clock pulse another data bit is pushed to the output. Through the transition of $\overline{CE}$ from "0" to "1" the data line returns to the high impedance state.

Reprogramming

In general, a full reprogramming operation consists of an erasure operation and a subsequent writing operation. During erase all bits of the selected word are set into the uniform "1" state, during writing "0" states are produced according to the information in the shift register.

A reprogramming operation is started when after data input and due to chip activation an information SB = "1" is in the relevant cell. Whether an erase or a writing operation is then taking place depends on the information that is on data line D during chip enable.

For erasure in state "1", a "1" must be present at the data input during transition of $\overline{CE}$ to low. If, however, a writing process is to be started in state "0", a "0" has to be present at the data line during chip enable.

Afterwards, a start pulse at the clock input Φ is required for the programming start. The control information has to remain stable at D until the leading edge of the start pulse is reached. The active data change starts with the trailing edge of this start pulse. The programming process is terminated by suppression of the chip enable, i.e. by $\overline{CE}$.

The reprogramming of a word is initiated with start and followed by an erase procedure. $\overline{CE}$ = "1" stops erasure. The control bit SB = "1" (in the shift register), which is also necessary for the write process, remains stable even after the termination of erasure. Thus, for writing the selected word, only the data line D has to be changed from "1" to "0", the chip has to be enabled again by $\overline{CE}$ = "0" and the data change has to be started by the start pulse.

An erase and a write process can also be executed separately. In order to obtain a safe "1" in all 8 bits of the selected memory address by the erase process, a data word is, however, to be entered with 8 times "1" before erasure. During the writing of a word which has not been erased before, the "0" states of the previous and the actual information are added.

Test Mode - Total Erasure

The test mode is activated, if the input TP (pin 7) is set from 0 V to 5 V = V_{DD}. To erase the entire memory, the test mode is to be turned on and the address 0 (A0 to A6) together with the control bit SB = 1 is to be entered. The subsequent program sequence is identical to the erasure of address 0. As soon as the erase procedure has terminated due to $\overline{CE}$ changing from 0 to 1, the test mode is to be turned off.

RESET

A memory which has not been selected is automatically in reset state by state $\overline{CE}$ = "1". All flipflops of the sequence control are reset. However, the information in the shift register is maintained and will only be changed by shifting the data. The reset state is also set in the case of the turning-on of the memory (power-on) by an on-chip circuit.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_{DD}	– 0.3	6	V
Input voltage	V_I	– 0.3	6	V
Power dissipation	P_D		40	mW
Storage temperature	T_{stg}	– 55	125	°C
Junction temperature	T_j		125	°C
Thermal resistance system - air	$R_{th\,SA}$		100	K/W

Operating Range

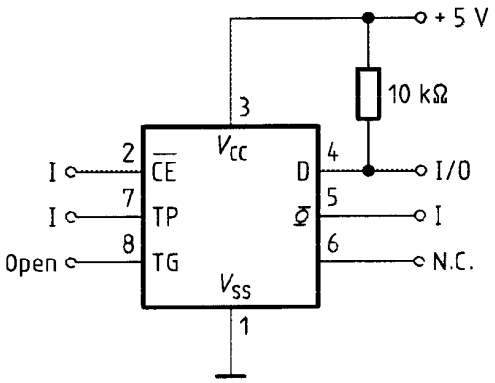
Supply voltage	V_{DD}	4.75	5.25	V
Ambient temperature	T_A	– 40	110	°C

Characteristics
T_A = 25 °C

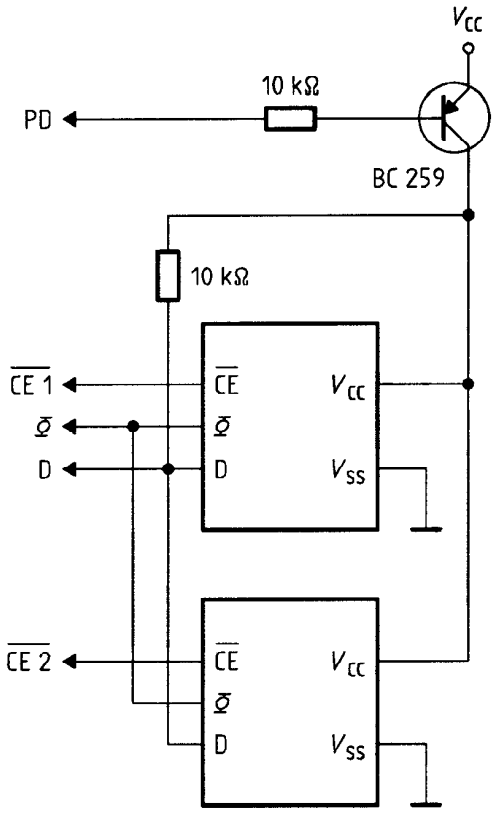
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply voltage	V_{DD}	4.75	5	5.25	V	
Supply current	I_{CC}			3	mA	V_{DD} = 5.25 V
Inputs						
Input voltage (D, Φ, $\overline{CE}$)	V_L			0.8	V	
Input voltage (D, Φ, $\overline{CE}$)	V_H	2.4			V	
Input current (D, Φ, $\overline{CE}$)	I_H			10	µA	V_H = 5.25 V

Characteristics (cont'd)
T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Data Output D (open drain)						
L-output current	I_L			0.5	mA	V_L = 0.8 V
H-output current	I_H			10	µA	V_H = 5.25 V
Clock Pulse Φ						
H-clock period	t_H	2.5		60	µs	
L-clock period	t_L	5			µs	
Edge spacing $\overline{CE}$ to D	Δt	2.5			µs	
Edge spacing $\overline{CE}$ to Φ	t_{AKT}	5			µs	
Data hold time (before/after Φ trailing edge)	t_{HD}	2.5			µs	
Data delay time (after Φ trailing edge)	t_{DD}	2.5			µs	
Rise time	t_r			1	µs	
Fall time	t_f			1	µs	
Chip erase duration	t_{er}	5		20	ms	
Write duration	t_{wr}	5		20	ms	
Full erasure duration	$t_{tot\ er}$	20		25	ms	



Test Circuit



Application Circuit

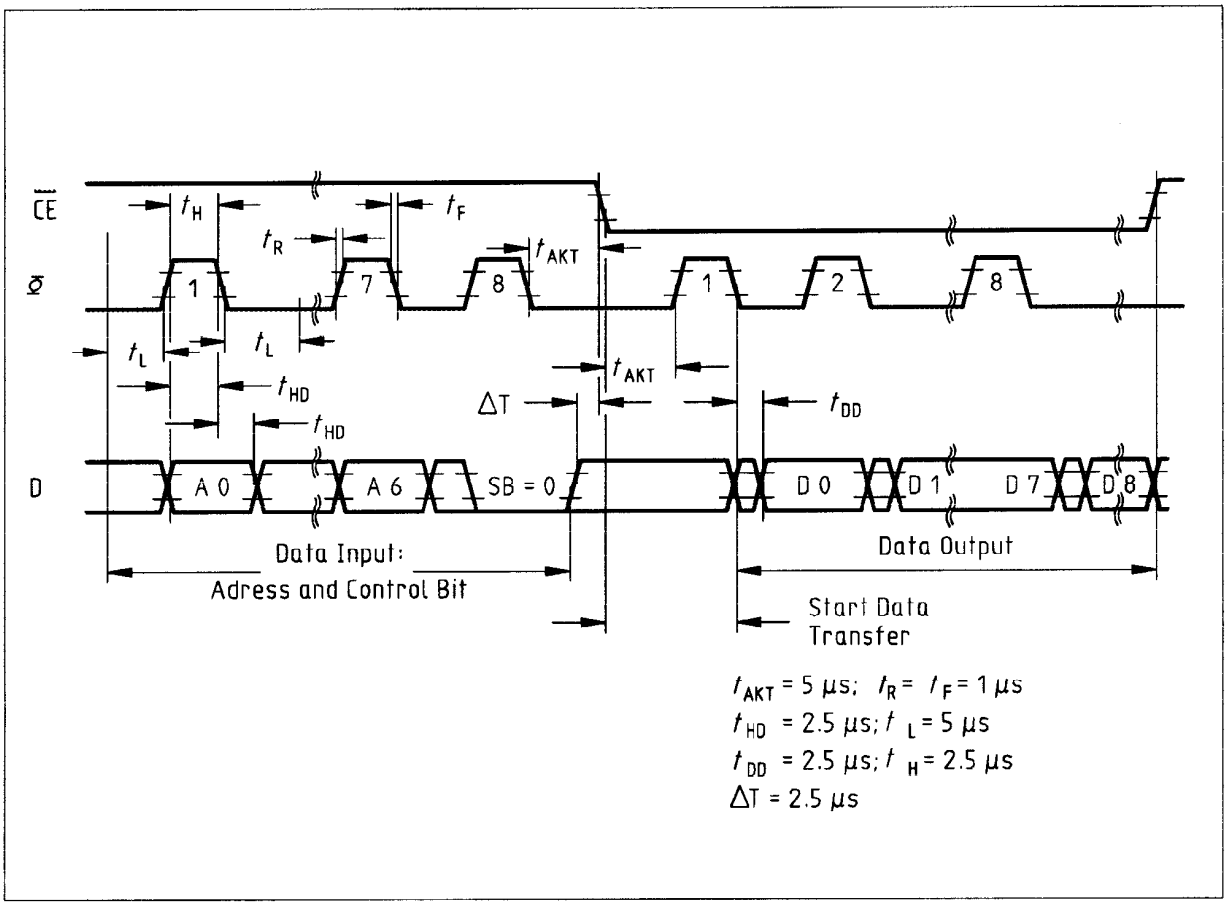


Diagram
Read

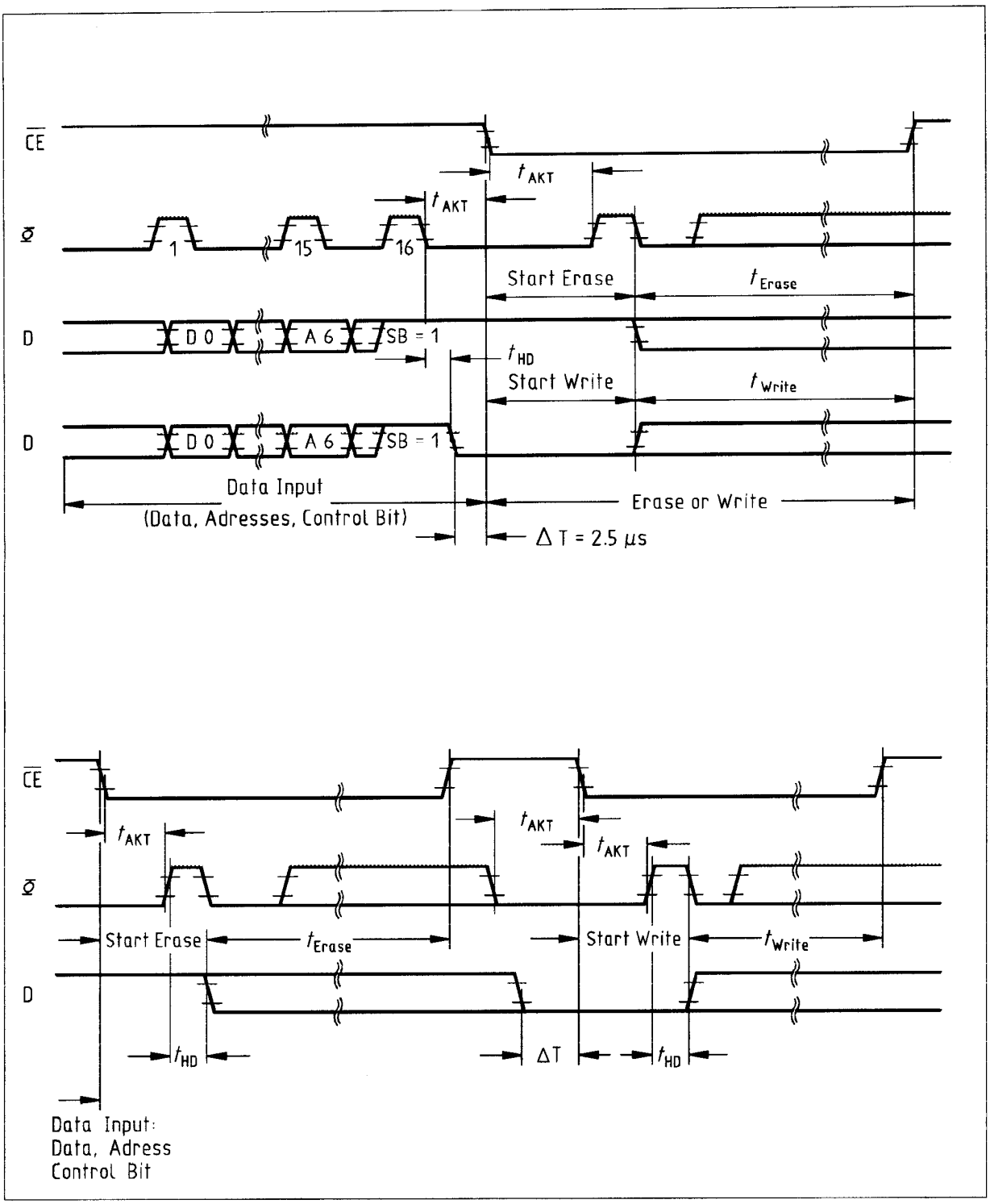


Diagram
Reprogramming